



PESD5V0S2BT

Low capacitance bi-directional double ESD protection diode in SOT23 package

Rev. 02 — 27 May 2004

Product data sheet

1. Product profile

1.1 General description

Low capacitance bi-directional double ESD protection diode in the small SOT23 plastic package designed to protect 2 data lines from the damage caused by Electro Static Discharge (ESD) and other transients.

1.2 Features

- Bi-directional ESD protection of 2 lines
- Low diode capacitance
- Max. peak pulse power: $P_{pp} = 130 \text{ W}$ at $t_p = 8/20 \mu\text{s}$
- Low clamping voltage: $V_{CL(R)} = 14 \text{ V}$ at $I_{pp} = 12 \text{ A}$
- Ultra low leakage current: $I_{RM} = 5 \text{ nA}$ at $V_{RWM} = 5 \text{ V}$
- ESD protection > 30 kV
- IEC 61000-4-2; level 4 (ESD)
- IEC-61000-4-5 (surge); $I_{pp} = 12 \text{ A}$ at $t_p = 8/20 \mu\text{s}$.

1.3 Applications

- Cellular handsets and accessories
- Portable electronics
- Computers and peripherals
- Communication systems
- Audio and video equipment.

1.4 Quick reference data

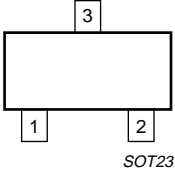
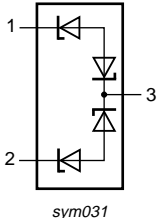
Table 1: Quick reference data

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-----------|---------------------------|---|-----|-----|-----|------|
| V_{RWM} | reverse stand-off voltage | | - | 5 | - | V |
| C_d | diode capacitance | $f = 1 \text{ MHz};$ $V_R = 0 \text{ V}$ | - | 35 | - | pF |
| | number of protected lines | | - | 2 | - | |

PHILIPS

2. Pinning information

Table 2: Discrete Pinning

| Pin | Description | Simplified outline | Symbol |
|-----|----------------|--|---|
| 1 | cathode 1 |  |  |
| 2 | cathode 2 | | |
| 3 | double cathode | | |

3. Ordering information

Table 3: Ordering information

| Type number | Package | | |
|-------------|---------|--|---------|
| | Name | Description | Version |
| PESD5V0S2BT | - | plastic surface mounted package; 3 leads | SOT23 |

4. Marking

Table 4: Marking

| Type number | Marking code ^[1] |
|-------------|-----------------------------|
| PESD5V0S2BT | *G5 |

- [1] * = p: made in Hong Kong.
 * = t: made in Malaysia.
 * = W: made in China.

5. Limiting values

Table 5: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol | Parameter | Conditions | Min | Max | Unit |
|------------------|-------------------------------|--------------------|--------|------|--------------|
| Per diode | | | | | |
| P_{pp} | peak pulse power | 8/20 μ s pulse | [1][2] | 130 | W |
| I_{pp} | peak pulse current | 8/20 μ s pulse | [1][2] | 12 | A |
| T_j | junction temperature | | - | 150 | $^{\circ}$ C |
| T_{amb} | operating ambient temperature | | -65 | +150 | $^{\circ}$ C |
| T_{stg} | storage temperature | | -65 | +150 | $^{\circ}$ C |

- [1] Non-repetitive current pulse 8/20 μ s exponential decay waveform; see [Figure 1](#).
 [2] Measured between pins 1 to 3 or pin 2 to 3.

Table 6: ESD maximum ratings

| Symbol | Parameter | Conditions | Value | Unit |
|--------|-------------------------------------|-----------------------------------|-----------|------|
| ESD | electro static discharge capability | IEC 61000-4-2 (contact discharge) | [1][2] 30 | kV |
| | | HBM MIL-Std 883 | 10 | kV |

[1] Device stressed with ten non-repetitive Electro Static Discharge (ESD) pulses; see [Figure 2](#).

[2] Measured between pins 1 to 3 or pin 2 to 3.

Table 7: ESD standards compliance

| Standard | Conditions |
|--|---------------------------------|
| IEC 61000-4-2; level 4 (ESD); see Figure 2 | > 15 kV (air); > 8 kV (contact) |
| HBM MIL-Std 883; class 3 | > 4 kV |

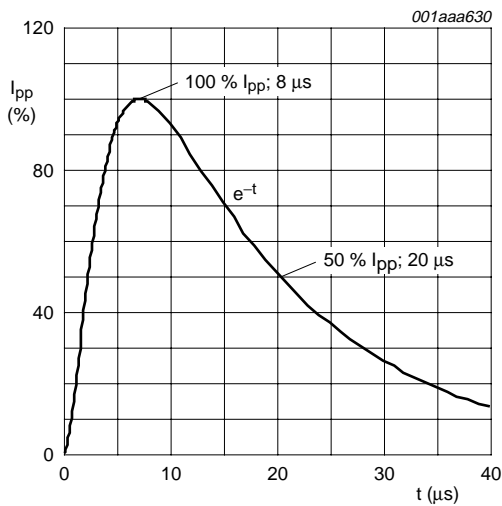


Fig 1. 8/20 μs pulse waveform according to IEC 61000-4-5.

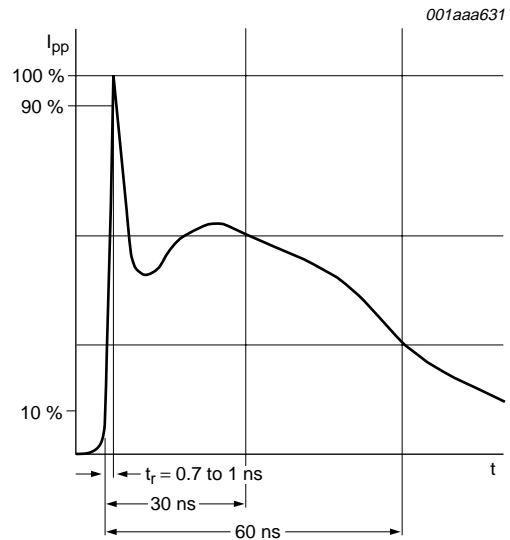


Fig 2. ElectroStatic Discharge (ESD) pulse waveform according to IEC 61000-4-2.

6. Characteristics

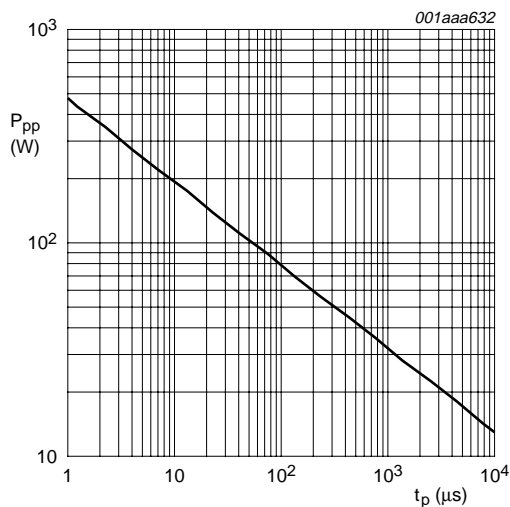
Table 8: Electrical characteristics

$T_{amb} = 25\text{ }^\circ\text{C}$ unless otherwise specified.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|------------------|---------------------------|--------------------------------------|--------|-----|-----|----------|
| Per diode | | | | | | |
| V_{RWM} | reverse stand-off voltage | | - | - | 5 | V |
| I_{RM} | reverse leakage current | $V_{RWM} = 5\text{ V}$ | - | 5 | 100 | nA |
| $V_{(CL)R}$ | clamping voltage | $I_{pp} = 1\text{ A}$ | [1][2] | - | 10 | V |
| | | $I_{pp} = 12\text{ A}$ | [1][2] | - | 14 | V |
| V_{BR} | breakdown voltage | $I_R = 1\text{ mA}$ | 5.5 | - | 9.5 | V |
| r_{diff} | differential resistance | $I_R = 1\text{ mA}$ | - | - | 50 | Ω |
| C_d | diode capacitance | $f = 1\text{ MHz}; V_R = 0\text{ V}$ | - | 35 | 45 | pF |

[1] Non-repetitive current pulse 8/20 μs exponential decay waveform, see [Figure 3](#).

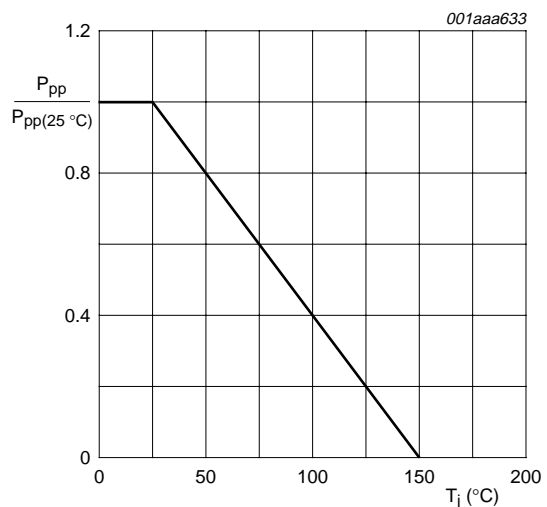
[2] Measured from pin 1 to 3 or pin 2 to 3.



$T_{amb} = 25\text{ }^\circ\text{C}$.

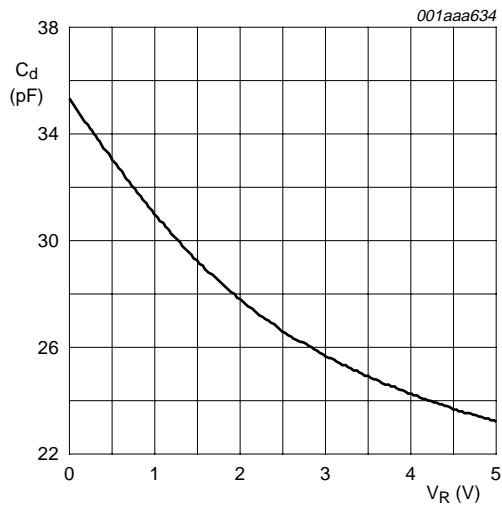
$t_p = 8/20\text{ }\mu\text{s}$ exponential decay waveform; see [Figure 1](#).

Fig 3. Peak pulse power dissipation as a function of pulse time; typical values.



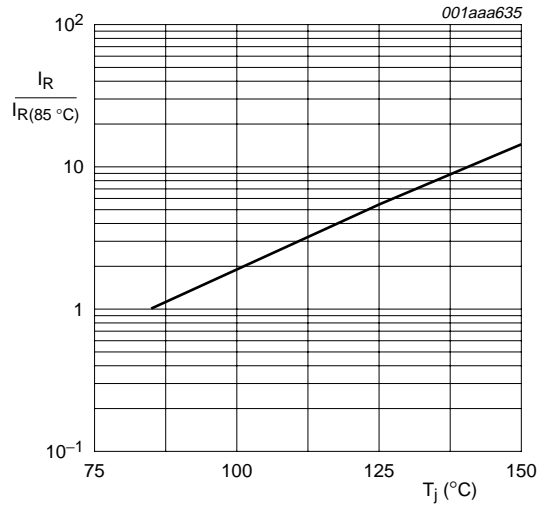
$T_{amb} = 25\text{ }^\circ\text{C}$.

Fig 4. Relative variation of peak pulse power as a function of junction temperature; typical values.



$T_{amb} = 25\text{ }^\circ\text{C}$; $f = 1\text{ MHz}$.

Fig 5. Diode capacitance as a function of reverse voltage; typical values.



$I_R < 1\text{ nA}$ measured at $T_{amb} = 25\text{ }^\circ\text{C}$.

Fig 6. Relative variation of reverse leakage current as a function of junction temperature; typical values.

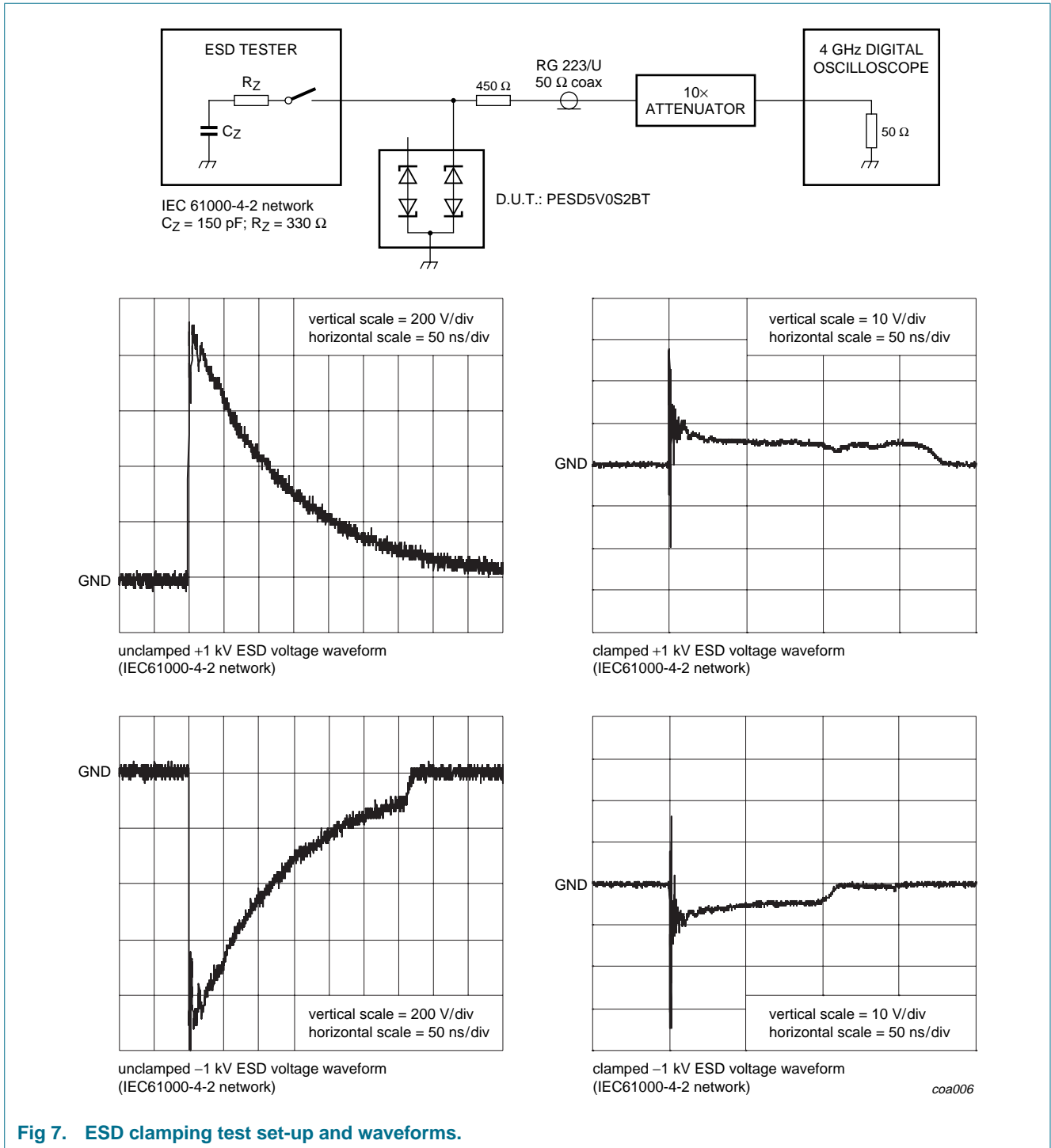


Fig 7. ESD clamping test set-up and waveforms.

7. Application information

The PESD5V0S2BT is designed for the bi-directional protection of 2 lines from the damage caused by Electro Static Discharge (ESD) and surge pulses. The PESD5V0S2BT may be used on lines where the signal polarities are above and below ground. The PESD5V0S2BT provides a surge capability of 130 Watts peak P_{pp} per line for an 8/20 μ s waveform.

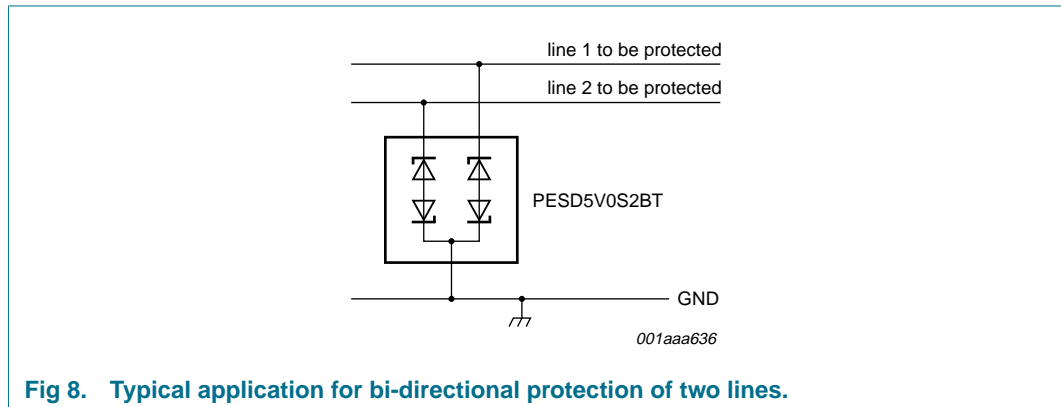


Fig 8. Typical application for bi-directional protection of two lines.

Circuit board layout and protection device placement:

Circuit board layout is critical for the suppression of ESD, Electrical Fast Transient (EFT) and surge transients. The following guidelines are recommended:

1. Place the PESD5V0S2BT as close to the input terminal or connector as possible.
2. The path length between the PESD5V0S2BT and the protected line should be minimized.
3. Keep parallel signal paths to a minimum.
4. Avoid running protected conductors in parallel with unprotected conductors.
5. Minimize all printed-circuit board conductive loops including power and group loops.
6. Minimize the length of the transient return path to ground.
7. Avoid using shared transient return paths to a common ground point.
8. Ground planes should be used whenever possible. For multilayer printed-circuit boards, use ground vias.

8. Package outline

Plastic surface mounted package; 3 leads

SOT23

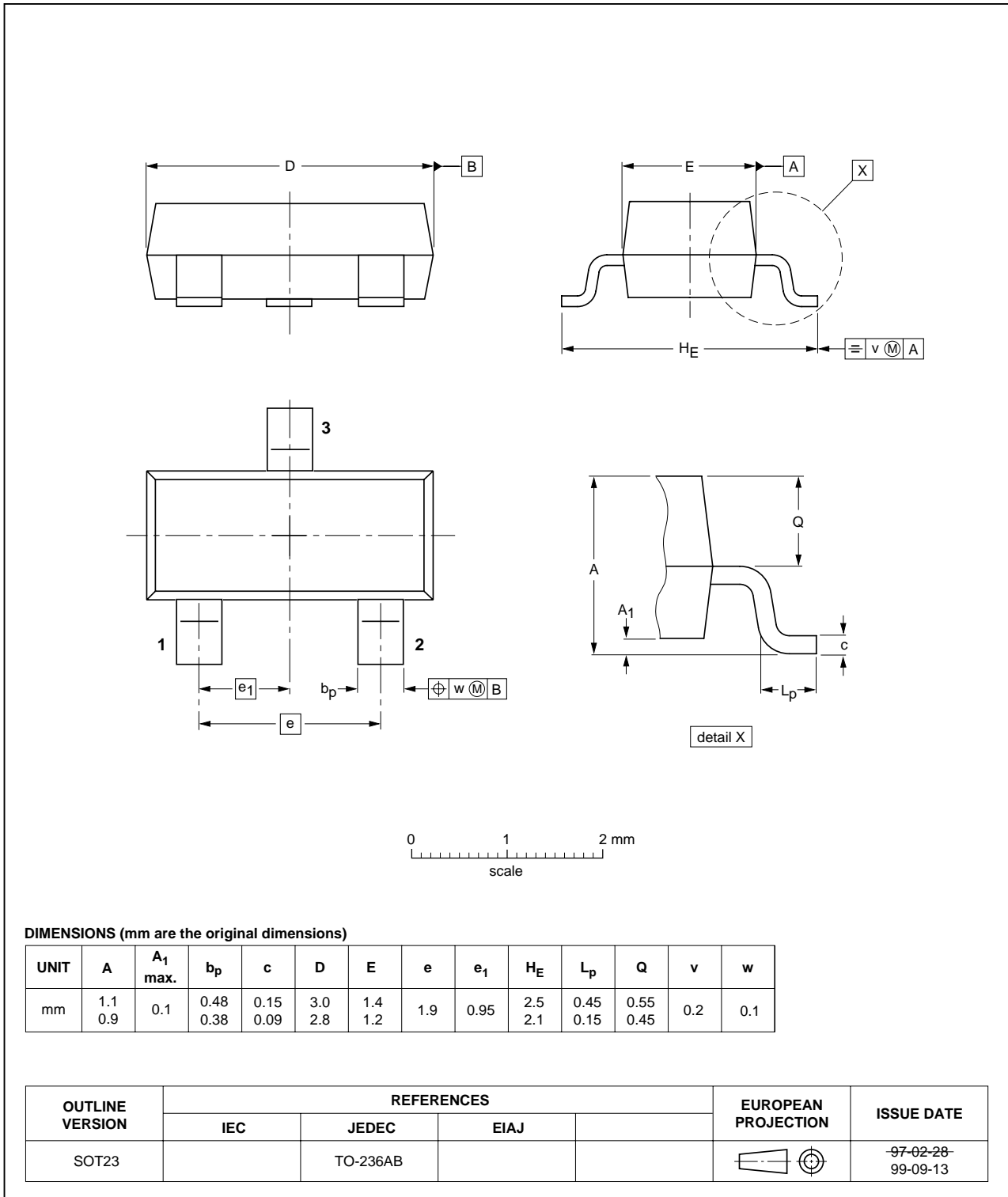


Fig 9. Package outline.

9. Revision history

Table 9: Revision history

| Document ID | Release date | Data sheet status | Change notice | Order number | Supersedes |
|---------------|--------------|-------------------|---------------|----------------|---------------|
| PESD5V0S2BT_2 | 20040527 | Product data | - | 9397 750 13344 | PESD5V0S2BT_1 |
| PESD5V0S2BT_1 | 20040517 | Product data | - | 9397 750 12901 | - |

10. Data sheet status

| Level | Data sheet status ^[1] | Product status ^[2] ^[3] | Definition |
|-------|----------------------------------|--|--|
| I | Objective data | Development | This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice. |
| II | Preliminary data | Qualification | This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product. |
| III | Product data | Production | This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN). |

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

11. Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information — Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors make no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

12. Disclaimers

Life support — These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips Semiconductors customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips Semiconductors for any damages resulting from such application.

Right to make changes — Philips Semiconductors reserves the right to make changes in the products - including circuits, standard cells, and/or software - described or contained herein in order to improve design and/or performance. When the product is in full production (status 'Production'), relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN). Philips Semiconductors assumes no responsibility or liability for the use of any of these products, conveys no license or title under any patent, copyright, or mask work right to these products, and makes no representations or warranties that these products are free from patent, copyright, or mask work right infringement, unless otherwise specified.

13. Contact information

For additional information, please visit: <http://www.semiconductors.philips.com>

For sales office addresses, send an email to: sales.addresses@www.semiconductors.philips.com

14. Contents

| | | |
|-----------|--------------------------------------|-----------|
| 1 | Product profile | 1 |
| 1.1 | General description | 1 |
| 1.2 | Features | 1 |
| 1.3 | Applications | 1 |
| 1.4 | Quick reference data | 1 |
| 2 | Pinning information | 2 |
| 3 | Ordering information | 2 |
| 4 | Marking | 2 |
| 5 | Limiting values | 2 |
| 6 | Characteristics | 4 |
| 7 | Application information | 7 |
| 8 | Package outline | 8 |
| 9 | Revision history | 9 |
| 10 | Data sheet status | 10 |
| 11 | Definitions | 10 |
| 12 | Disclaimers | 10 |
| 13 | Contact information | 10 |



© Koninklijke Philips Electronics N.V. 2004

All rights are reserved. Reproduction in whole or in part is prohibited without the prior written consent of the copyright owner. The information presented in this document does not form part of any quotation or contract, is believed to be accurate and reliable and may be changed without notice. No liability will be accepted by the publisher for any consequence of its use. Publication thereof does not convey nor imply any license under patent- or other industrial or intellectual property rights.

Date of release: 27 May 2004
Document order number: 9397 750 13344

Published in The Netherlands